



Lithography

2T307: Co-operation of photomask reticule supply chain for improved yield, secured time to market and added life time (CRYSTAL)



Improved photomask qualification cuts redesign and speeds time to market

Improving photolithography mask processing is crucial in view of ever shorter product lifetimes and to ensure devices get to market at the right time. Innovations in the CRYSTAL project included an international design-for-manufacturability methodology standard, integrated contamination control and a new photomask qualification procedure. Major outcomes were robust tools for immediate commercialisation and clear demonstration in critical use cases that integration in the design flow is risk free with many benefits. European chipmakers and their equipment suppliers are already exploiting the results.

Better control of photolithography is key to continuous improvement in semiconductor fabrication productivity. Photomask sets play an essential role in imaging performance and contribute strongly to costs, quality and yield of the process. With the extremely steep yield ramp-up now demanded, there is even less room for mask redesign as the profitable lifetime of a chip can be only three to six months. Short cycle times through the mask supply chain are crucial for early product availability.

While immersion techniques may be the only economic approach to extending current 193 nm wavelength lithography down to the 32 nm node for semiconductor devices, photomask technology is even more stressed by a series of new challenges. These include:

- Design interaction involved in Moore integration, mixing different functions on chip and thus varying optical densities in one lithography layer, while lacking efficient feedback loops to the design world;
- Molecular contamination from the high illumination energy required with deep ultraviolet immersion technology, a risk of shift and instability of process control of the extreme requirements for control of critical dimensions; and
- The dependency of the lithography process window on reticule enhancement techniques stability. This results in too much

complexity to manage process changes easily and unrealistic photomask qualification cycle times, penalising continuous improvement processes.

Three complementary areas

The MEDEA+ 2T307 CRYSTAL project set out to more than halve photomask production cycle time and reduce potential process deviation or excursion risks by at least 50%. The project involved chipmakers, their equipment and materials suppliers, and major research organisations.

CRYSTAL focused on boosting photomask manufacturability for 193 nm lithography in three complementary areas:

1. Photomask design for manufacturability (DfM)

Semiconductor designers are increasingly specialised and less aware about manufacturing. CRYSTAL focused on automating links between design and lithography; it developed a set of rules and the way they should be used. The rules are structured in seven groups, each with a different optimisation. All the designer has to do is to select the rule required. This should eradicate 90 to 95% of electronic design automation (EDA) errors. The set of XML-level rules and associated methodology have been standardised in the IEEE. French partner Satin IP has developed

the VIP Lane design quality monitoring and closure tool which enables checking to ensure the right rules are observed.

2. Molecular contamination control

A high level of energy is fed into the photomask during the lithography projection process, resulting inevitably in contamination. This is compounded by humidity. CRYSTAL worked with academics to obtain the scientific understanding of the chemical and physical mechanisms involved.

The resulting knowledge of the organic and inorganic contamination concerned on both sides of the mask made it possible to adapt the materials and coatings involved, improve the cleaning processes – particularly through the use of vacuum conditions – and develop totally new tools and concepts to meet the even more demanding requirements of the next generation of mask production.

3. Photomask qualification procedures

Existing metrology was not necessarily ideal for linking the lithography process to specific changes in final test on wafer. Rather than developing a new set of metrology, it was felt better to reuse existing metrology sites in the industry standard OPUS approach which offers a model for each technology based on a test mask with 14 families of test sites. The outcome is a test signature which indicates what process corrections are required. This well-known approach demonstrated that the new CRYSTAL process worked well with changes having no effect on wafer process. Developing the right metrology was time consuming, including adapting to the aerial image measurement system (AIMS).

Some 90% of the technical problems were solved within the project as planned. This work will be continued and expanded between several partners now the project has finished.

Speeding mask production

This project demonstrated a reduction of cycle-time excursion risks by 57% – about 11 weeks – while cutting photomask qualification cycle time by 25 to 88%, depending on the qualification and technology nodes involved. Expectations are to improve related metrics by 50%. CRYSTAL also initiated an international standard in IEEE to facilitate integration of DfM rules in the EDA flow.

Exploitation has started. While the IEEE standardisation of photomask DfM rules has inevitably taken time, the approach is already used by project partners with the necessary software incorporated into commercial enterprise solutions. The molecular contamination cleaning process has been proved and the knowledge has been widely disseminated; relevant tools have also been developed and are being marketed. Finally, tools for the proposed improved photomask qualification process have also been developed and are ready for commercialisation.

Xyalis and Satin have implemented the DfM module in Gtmodus and VIP lane software, Entegris Cleaning Process uses the contamination knowledge to improve pod cleaning, STMicroelectronics has implemented Alcatel pod-cleaning tools, Carl Zeiss AIMS 45 is a market standard aerial image tool, Advanced Mask Technology Center and Toppan deliver ppb level contaminated photomasks and can monitor single changes in material and processes through a 193 nm test bench.



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Advanced Mask Technology Center
Alcatel Vacuum Technology
ASML
Atmel
Carl Zeiss SMS
CEA-LETI
DMS
Entegris Cleaning Process
Fraunhofer Institute IISB
LTM-CNRS
Satin IP
STMicroelectronics
Toppan Photomasks France
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KEY PROJECT DATES:

Start: January 2008
End: December 2010

COUNTRIES INVOLVED:

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Germany
The Netherlands



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